Notice of Allowability	Application No.	Applicant(s)	
	09/612,582	NARAHARA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *October 11, 2005*.

2. ☒ The allowed claim(s) is/are *25 and 31*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated October 11, 2005. Claims 1-24 and 26-30 were cancelled. Claim 25 was amended. Claim 31 was added. Claims 25 and 31 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Robert Bodi on November 25, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In the claims:

In the amended Claim 25, Lines 14-15, "wherein the modeling step includes a triangular waveform modeling step"

has been changed to

-- a triangular waveform modeling step--.

In Claim 31, Lines 2-5, "wherein the triangular waveform modeling step of further modeling the change arising in an event as a center of an isosceles triangle"

has been changed to

-- wherein the triangular waveform is an isosceles triangle, wherein an event occurs at the center of the width of the isosceles triangle, and wherein the width is the base of the isosceles triangle --.

Reasons for Allowance

4. Claims 25 and 31 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) power line conducting noise is the main source of EMI in LSIs; the EMI is caused by high frequency current, which in turn is caused by chip switching activities; modeling the on-chip switching activities and performing circuit simulation to obtain current waveform outgoing from chip through power/ground ports; on-chip capacitance between power and ground wires plays important role in EMI analysis; the simulation provides spectrum analysis result; switching

current consumed in the blocks is simulated assuming ideal power supply voltage first; then the circuit simulation is performed for power network to which current sources representing switching current waveform of circuit blocks are attached; the switching current waveform can be obtained using logic simulator and cell switching current waveform library; switching current waveform in the library are superposed to each event when the cell switches; then the current waveforms for each event are obtained; the switching current wave changes depending on the input slew and output load; the current waveforms for various input slew and output load are stored in the library; the intermediate slew and load values are obtained by interpolation; the waveforms are stored as triangular waveform to minimize the amount of data to be stored; voltage drops occur during switching activity; then the current waveforms deviate; the voltage drop data is then back annotated into the current waveform extraction step; by performing the Fast Fourier transform for current waveforms, the noise spectrum is obtained (**Hayashi et al.,** "EMI-Noise Analysis under ASIC design environment", ACM 1999);

(2) analyzing on-chip power supply noise for high performance microprocessors; power supply noise is cause by the switching current; excessive noise causes additional signal delay and false switching of logic gates; on-chip decoupling capacitors are used to keep the power supply within specification and provide signal integrity and reduce EMI radiation noise; the switching noise is caused by changes in current through various parasitic inductors; the simultaneous switching of I/O drivers and internal circuits can increase the voltage drop of the power supply; maximum noise occurs during switching when the current change is maximum; an integrated package level and chip level power bus model with switching and timing information is used to accurately analyze the voltage variation with time; an iterative improvement procedure

is used to estimate the on-chip decoupling capacitance needed; in the model, the non-linear devices and capacitive loads are replaced with piecewise linear current sources, which mimic the waveform of the actual circuits; a triangular or trepezoidal waveform can be obtained by calculating the total average current and peak current for each cell (**Chen et al.,** "Power supply noise analysis methodology for Deep-submicron VLSI chip design", ACM 1997); and

(3) a method and apparatus for accurately estimating signal delays of an electrical circuit, taking into account both the resistance and capacitance of an interconnect network; modeling the gate to provide gate delay estimates taking into account slew time of the input signals; obtaining an estimate of total gate delay and an estimate of gate output slew time using a gate timing model; producing an estimated network output delay as a function of output network resistance and estimated gate driving strength; using the output network delay and an estimated gate output slew time to produce an estimated destination point slew time at one or more destination points; the output slew time is an estimate of the slope of the voltage as a function of time waveform produced on the output network of the interconnect; producing an output slew time for a gate assuming a lumped capacitance to be the sole load of a gate; using estimated gate delay and estimated output slew time of a gate to calculate an estimated driving strength using the load characteristic of the output network (**Spyrou et al.,** U.S. Patent 5,841,672).

Additional state of the art reviewed and considered by the Examiner is found in U.S. Patent 6,959,250; U.S. Patent 6,876,210; U.S. Patent 6,810,340; U.S. Patent 6,782,347; U.S. Patent 6,754,598; U.S. Patent 5,852,445; U.S. Patent 5,959,481; U.S. Patent 6,687,205; U.S.

Patent 6,278,964; U.S. Patent 6,242,951; U.S. Patent Application 2004/0117169; U.S. Patent Application 2004/0232962.

None of these references taken either alone or in combination with the prior art of record discloses an electromagnetic interference analysis method for analyzing the amount of electromagnetic interference arising in an LSI by means of performing a gate level simulation, specifically including:

"a triangular waveform modeling step of modeling the instantaneous current as a triangular waveform whose width is calculated from each event information in consideration of output slew information for an output terminal of a cell for each event information such that the area of the triangular waveform becomes equal to the amount of electric current of each event, the height of the triangular waveform being calculated on the basis of the width".

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
November 26, 2005

Paul L. Rodriguez 11/28/05
Primary Examiner
Art Unit 2125